

Electrical Characteristics at T_j
Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\text{ A}$	150	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\text{ A}$	1	2.1	3	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=150V, T_j$	-	-	1	A
		$V_{GS}=0V, V_{DS}=150V, T_j$	-	-	100	
Gate to Source Leakage Current	I_{GSS}	$V_{GS} \quad V_{DS}=0V$	-	-	100	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$	-	58	65	m
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=5A$	-	66	82	m
Transconductance	g_{fs}	$V_{DS}=5V, I_D=10A$	-	25	-	S
Gate Resistance	R_G	$V_{GS}=0V, V_{DS}\text{ Open}, f=1\text{MHz}$	-	3.90	-	

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=75V, f=1\text{MHz}$	-	635	-	pF
Output Capacitance	C_{oss}		-	43	-	
Reverse Transfer Capacitance	C_{rss}		-	4.3	-	
Total Gate Charge	$Q_g(10V)$	$V_{DD}=75V, I_D=10A, V_{GS}=10V$	-	8.2	-	nC
Total Gate Charge	$Q_g(4.5V)$		-	3.7	-	
Gate to Source Charge	Q_{gs}		-	2.3	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	0.8	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=75V, I_D=10A, V_{GS}=10V, R_G=10\text{ }\Omega$	-	8	-	ns
Rise time	t_r		-	4	-	
Turn off Delay Time	$t_{d(off)}$		-	12	-	
Fall Time	t_f		-	3	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_F=20A$	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$V_R=75V, I_F=10A, di_F/dt=100A/\text{s}$	-	48	-	ns
Reverse Recovery Charge	Q_{rr}		-	54	-	nC

Fig 1. Typical Output Characteristics

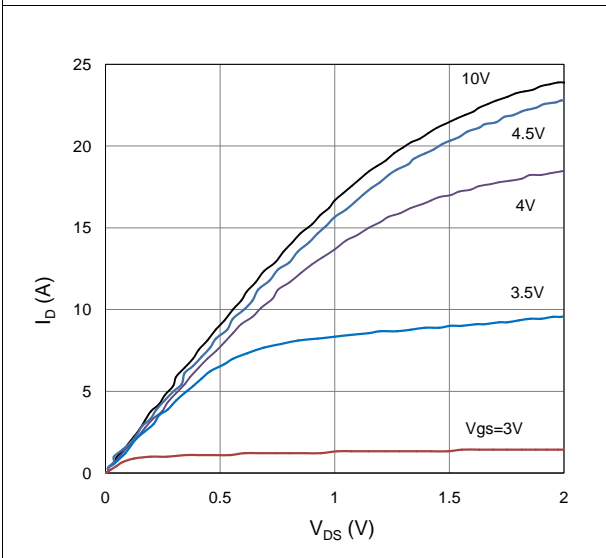


Figure 2. On-Resistance vs. Gate-Source Voltage

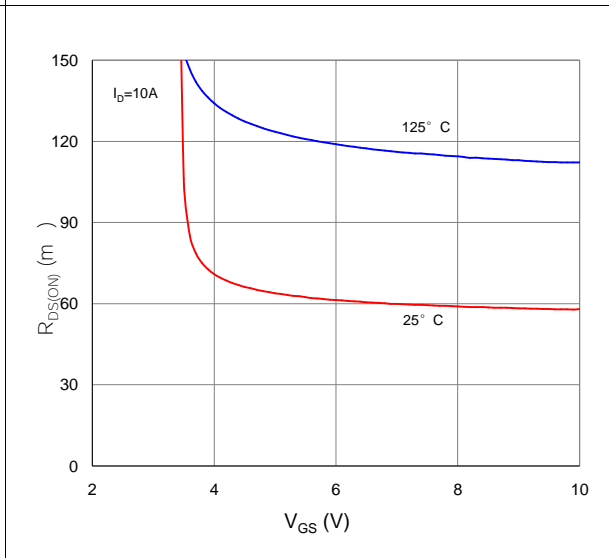


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

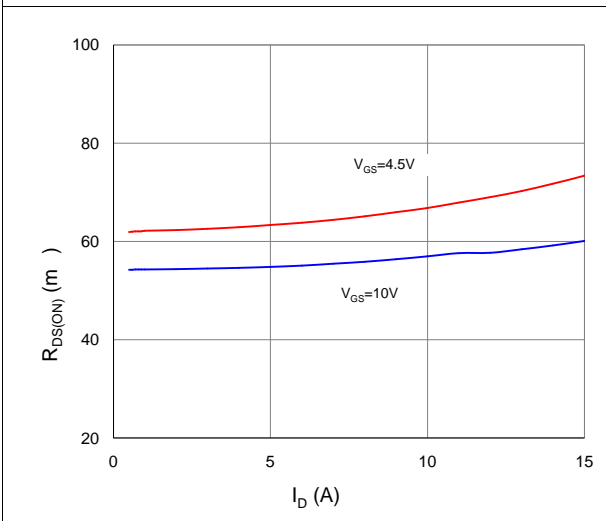


Figure 4. Normalized On-Resistance vs. Junction Temperature

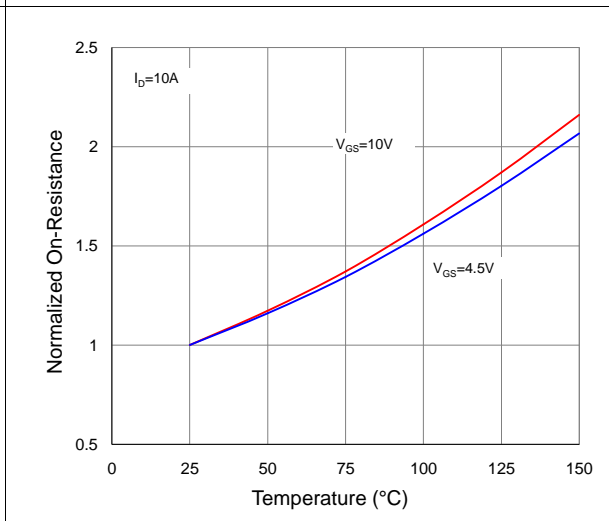


Figure 5. Typical Transfer Characteristics

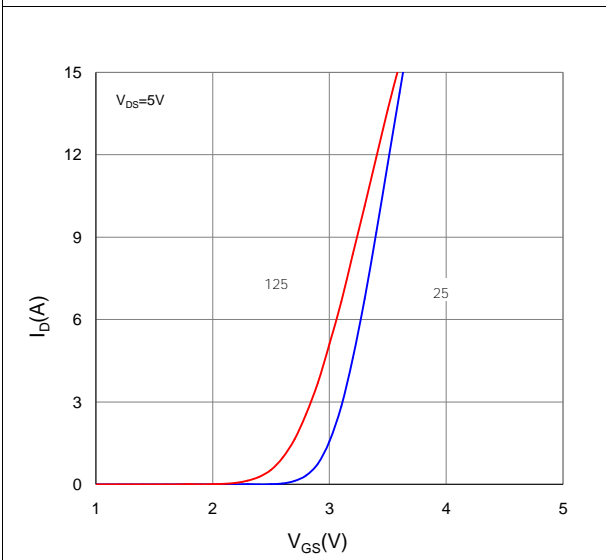


Figure 6. Typical Source-Drain Diode Forward Voltage

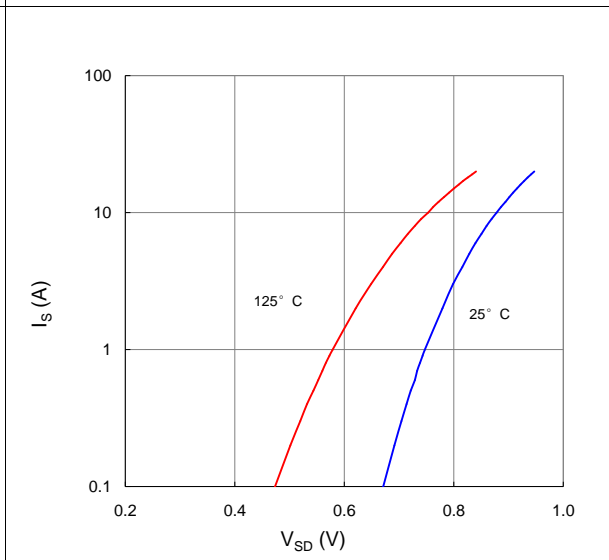


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

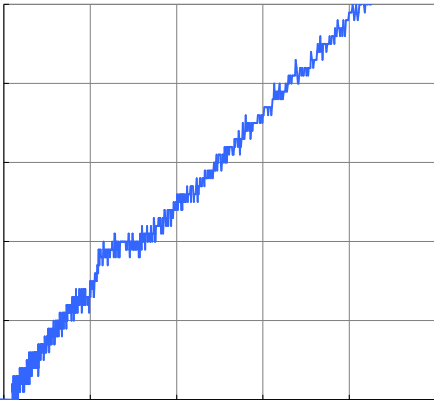


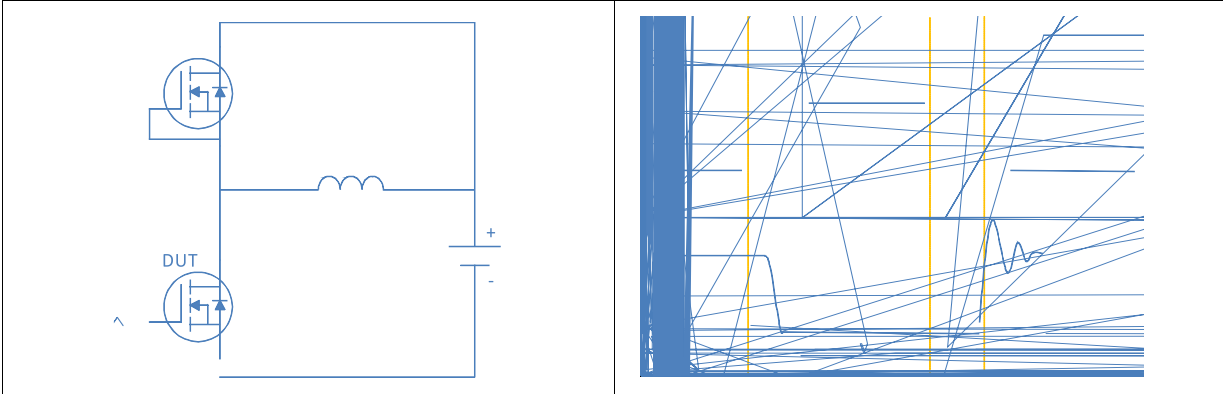
Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

Figure 9. Maximum Safe Operating Area

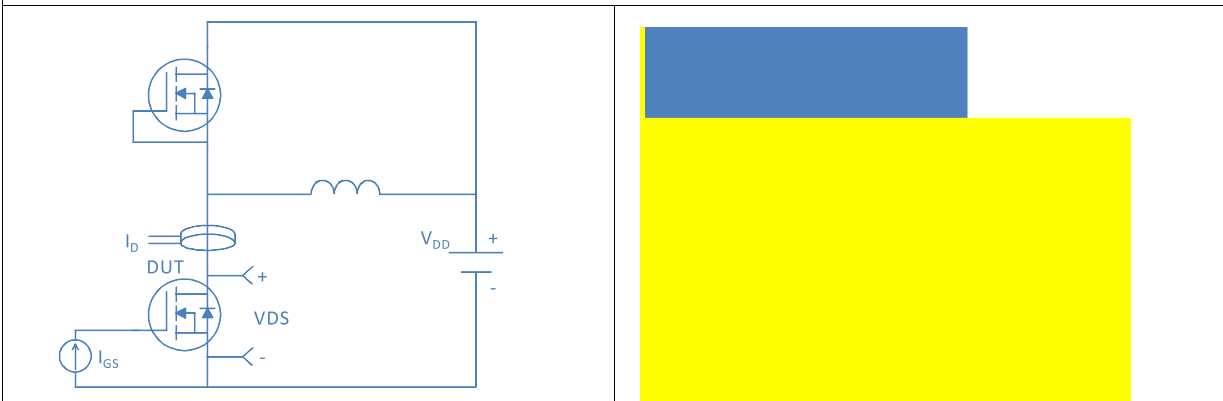
Figure 10. Maximum Drain Current vs. Case Temperature

Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

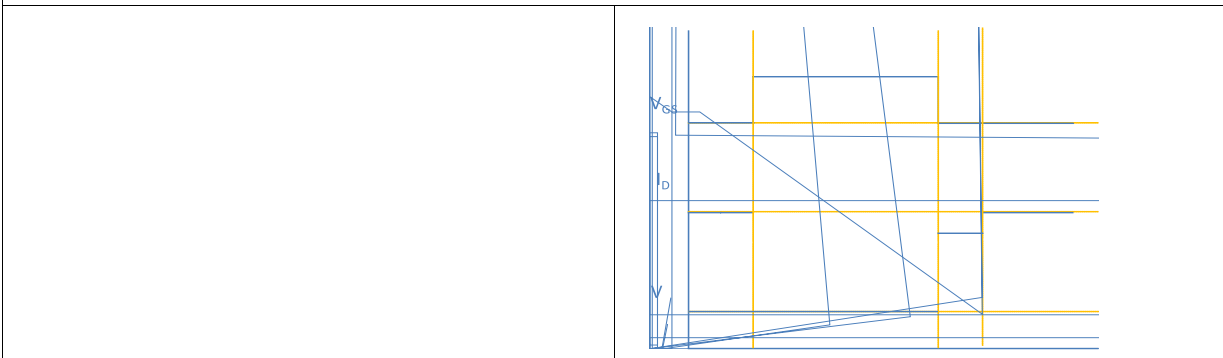
Inductive switching Test



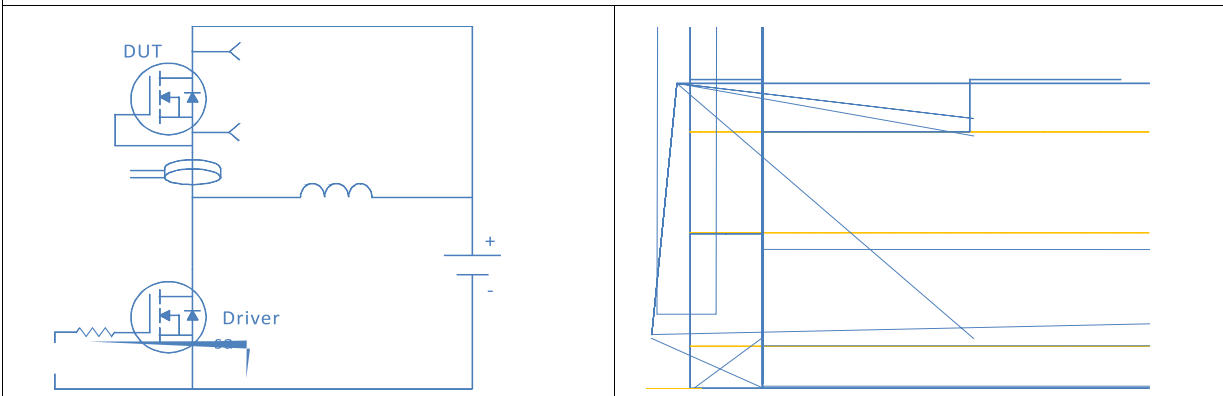
Gate Charge Test



Uclamped Inductive Switching (UIS) Test

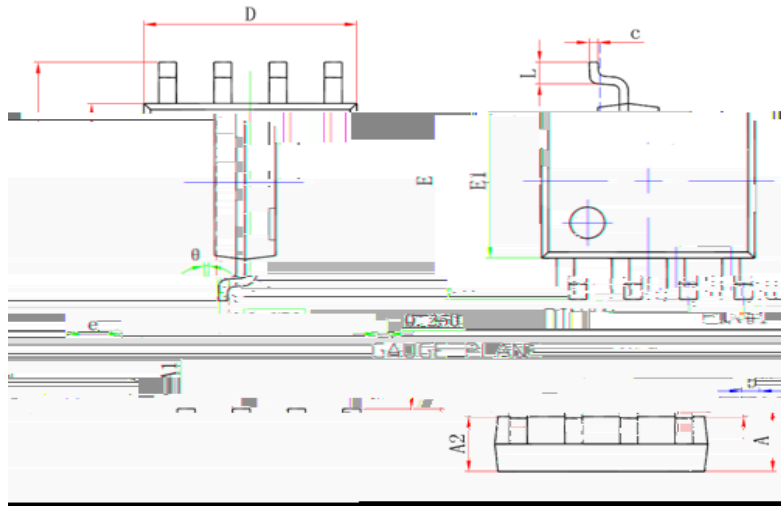


Diode Recovery Test



Package Outline

SOIC-8, 8 leads



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (SBC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.031
theta	0°	8°	0°	8°